Design of a model predictive controller for the dual-active bridge converter

Marco Guerreiro, Wesley Becker, Pedro dos Santos, and Steven Liu
Chair of Control Systems, RPTU University Kaiserslautern-Landau, Kaiserslautern, Germany
Corresponding author: marco.guerreiro@rptu.de

***Abstract*—This paper explores continuous control set model predictive control (CCS-MPC) for voltage control of the dual-active bridge (DAB), including constraints on the phase-shift and the transformer peak-to-peak current. We show a feasible real-time implementation of long-horizon CCS-MPC, leading to a dynamic voltage controller suited for grid-forming operation of the DAB converter.**

***Index Terms*—model predictive control, converter control, dual-active bridge, optimal control.**

I. Introduction

Advances in power electronics, the drive towards renewable energy generation and the shift from centralized to distributed generation have made dc microgrids a promising element of the next-generation power system [1], [2]. One key feature of dc microgrids is their ability to operate in islanded mode, i.e. isolated from the main grid. In this scenario, the microgrid supplies its loads with local generation, increasing supply reliability in cases of disruptions in the main grid.

One of the challenges in islanded dc microgrids is stabilizing the dc bus. During islanded operation, units inside the microgrid must maintain the voltage on the main bus, a process called grid-forming [3], [4]. At low level, grid-forming units work in voltage mode and stabilize the dc bus by balancing generation and demand within the grid. To prevent oscillations in the bus, it is important that these units present a dynamic voltage response in the presence of load and setpoint changes, a challenging task as nowadays most loads have an interfacing converter and behave as constant power loads (CPLs).

One converter topology gaining increasing attention as a grid-forming unit is the dual-active bridge (DAB), due to its characteristics such as galvanic isolation, bidirectional power flow, and possibility of soft switching [5], [6]. Therefore, it is important to develop advanced voltage control strategies for the DAB converter that are able to show dynamic response while respecting physical constraints of the converter. A well suited control strategy for such problem is model predictive control (MPC), an optimization-based strategy that has been successfully employed in many industrial applications [7]. The main drawback of MPC is its high computational cost, which in the past has limited its use for systems with slow dynamics. However, advances in microprocessor technology have now made it possible to use MPC for systems with real-time constraints in the sub-millisecond range, enabling use of MPC for power converter control [8].

MPC has been previously proposed for voltage control of the DAB [9]–[15]. Most of the previously reported approaches have focused on single-step prediction horizons, with a cost function without penalty terms on the control signal. These approaches generally lead to controllers resembling dead-beat control that, although highly dynamic, are very aggressive and more susceptible to noise. Moreover, short prediction horizons can introduce additional oscillations that longer horizons would otherwise prevent.

This paper explores long horizon, continuous-control set MPC (CCS-MPC) for voltage control of the DAB converter. The formulation of the problem assumes the reduced-order model of the DAB under single phase shift (SPS) modulation. Control weighting factors are included in the optimization problem, and two types of constraints are considered: on the phase shift, and on the peak-to-peak current of the transformer. In order to achieve a feasible real-time implementation of the controller, different control and switching frequencies are used. In this way, the real-time constraint of the controller is alleviated, while the switching frequency remains the one designed for the converter. In order to check real-time feasibility, the controller is verified using a processor-in-the-loop (PiL) scheme, where the converter is simulated in a computer, and the controller is executed in a real-time target [16]. The main result of this paper is the implementation of a constrained, long horizon CCS-MPC controller for a 50 kHz DAB.

The rest of this paper is organized as follows. Section II discusses the formulation of the control problem, including constraints on the phase shift and transformer peak-to-peak current. Section III shows the simulation results, discussing the design of the controller for different control frequencies. Section IV concludes this paper.

II. Constrained Model Predictive Control of the DAB

A. Model

The DAB converter is shown in Fig. 1, where V_i is the input voltage (primary side), V_o is the output voltage (secondary side), L_lk is the leakage inductance, and C_o is the output capacitor. The primary and secondary sides are isolated through a high-frequency transformer with turns ratio $N = \mathrm{N_p}/\mathrm{N_s}$, and switches $S_1, S_2, \cdots, S_8$ are used to control the full bridges of each side. The current i_R is the current that is rectified from the full bridge of the secondary side, I_o is the current of the load, and i_L is the current through L_lk.

 DOI 10.1109/ICDCM63994.2025.11144644

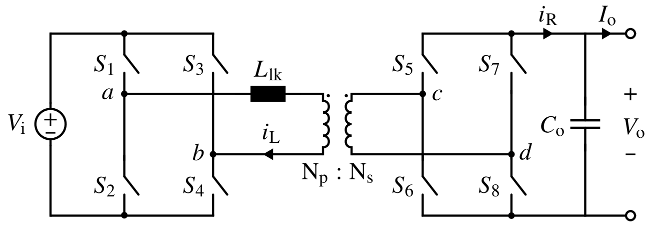

Fig. 1. Dual-active bridge converter.

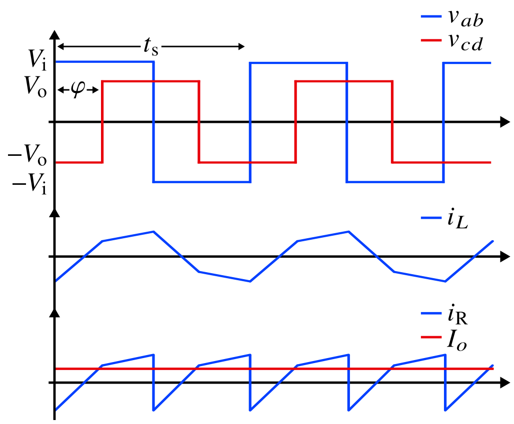

Fig. 2. Steady-state waveforms for the dual-active bridge converter.

In this paper, it is assumed that the DAB is controlled using SPS modulation. In this modulation, each full bridge is operated with a 50% duty-cycle, fixed switching period t_s, and a phase shift φ is introduced between the two bridges ($-0.25 < \varphi < 0.25$). The waveforms for the voltages v_{ab} and v_{cd}, and currents i_L, i_R and I_o are shown in Fig. 2.

In steady-state, the average I_R of the rectified current i_R is equal to the output current I_o and is given by [17]

$$I_R = \left(\frac{NV_i t_s}{L_{lk}}\right)(1 - 2|\varphi|)\,\varphi. \tag{1}$$

Moreover, the peak-to-peak current through the leakage inductance is

$$I_{L,pk\text{-}pk} = \left(\frac{t_s}{2L_{lk}}\right)\big(V_i - (1 - 4\varphi)\,NV_o\big). \tag{2}$$

For control design purposes, the reduced-order model of the DAB converter is used [18]. In this model, the dynamics of the current of the leakage inductor is assumed to be much faster than that of the output capacitor, such that it is possible to assume that changing the phase-shift φ directly controls the average rectified current I_R. The resulting model is illustrated in Fig. 3, where $i(t)$ represents a controllable current source, and the load is represented by a current sink with current $i_o(t)$. The current $i(t)$ is controlled by manipulating φ, and the relationship between $i(t)$ and φ is given by (1). The dynamics of the output voltage of the DAB is then given by

$$C_o\dot{v}_o(t) = i(t) - i_o(t). \tag{3}$$

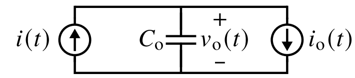

Fig. 3. Reduced-order model of the dual active bridge.

B. Control problem formulation

Next, the control problem is formulated as an optimization problem, where the objective is to simultaneously minimize the error between the output voltage and a reference signal, and the rate of change of the phase shift. First, model (3) is discretized using forward Euler and augmented with an integrator, leading to the discrete-time state-space model [19]

$$x(k+1) = Ax(k) + B\Delta u(k), \tag{4a}$$
$$y(k) = Cx(k), \tag{4b}$$

where $x(k) = \begin{bmatrix} v_o(k) - v_o(k-1) & y(k)\end{bmatrix}^\intercal$, $\Delta u(k) = u(k) - u(k-1)$, $u(k) = i(k)$, $y(k) = v_o(k)$, and

$$A = \begin{bmatrix}1 & 0\\ 1 & 1\end{bmatrix},\ B = \begin{bmatrix}t_d/C_o\\ t_d/C_o\end{bmatrix},\ C = \begin{bmatrix}0 & 1\end{bmatrix}, \tag{5}$$

where $t_d \le t_s$ is the discretization period, and is the same as the control (sampling) period. The cost function of the optimization problem is formulated as

$$J = \sum_{i=k_i}^{k_i+N-1} \big(r(i+1) - y(i+1)\big)^2 + r_w\big(\Delta u(i)\big)^2, \tag{6}$$

where N is the prediction horizon, k_i is the sampling instant and r_w is a weighting factor. Writing the cost term (6) as a function of the input, initial state and system matrices leads to the standard quadratic programming (QP) formulation

$$\begin{aligned}\min_{\Delta U}\quad & J = \frac{1}{2}\Delta U^\intercal H \Delta U + \Delta U^\intercal K,\\ \text{s.t.}\quad & M\Delta U \le \gamma,\end{aligned} \tag{7}$$

where $\Delta U = \begin{bmatrix}\Delta u(k_i) & \cdots & \Delta u(k_i+N-1)\end{bmatrix}^\intercal$, $H = \Phi^\intercal\Phi + R_w$, $K = -\Phi^\intercal\big(R - Fx(k_i)\big)$, and M and γ represent the inequality constraints. Moreover, $R_w = r_w I_{N\times N}$ and $R = \begin{bmatrix}r(k_i+1) & \cdots & r(k_i+N)\end{bmatrix}^\intercal$. Matrices Φ and F result from the model and are defined as in [19].

C. Formulation of the constraints

Matrix M and vector γ, which represent the inequality constraints, can be defined by referring to model (3). In this model, the current source i is the input signal and is assumed to be equal to the average of the rectified current (I_R). The bounds for this current can be defined based on the limits of the phase shift or the peak-to-peak current of the transformer.

1) Constraints based on phase shift limitation: The rectified current I_R is bounded by the phase-shift φ according to (1), which is physically bounded by $\varphi \in (-0.25, 0.25)$ but in practice it might be desired to set tighter bounds. Thus, if $\varphi \in (\varphi_{\min}, \varphi_{\max})$, the current source i is bounded by

$$i_{\min} \geq \left(\frac{NV_{\mathrm{i}}t_{\mathrm{s}}}{L_{\mathrm{lk}}}\right)(1-2|\varphi_{\min}|)\,\varphi_{\min}, \tag{8a}$$

$$i_{\max} \leq \left(\frac{NV_{\mathrm{i}}t_{\mathrm{s}}}{L_{\mathrm{lk}}}\right)(1-2|\varphi_{\max}|)\,\varphi_{\max}. \tag{8b}$$

The inequality constraint can then be written as

$$\begin{bmatrix} -u(k_i) \\ -u(k_i+1) \\ \vdots \\ -u(k_i+N_{\mathrm{c}}-1) \\ u(k_i) \\ u(k_i+1) \\ \vdots \\ u(k_i+N_{\mathrm{c}}-1) \end{bmatrix} \leq \begin{bmatrix} -i_{\min} \\ -i_{\min} \\ \vdots \\ -i_{\min} \\ i_{\max} \\ i_{\max} \\ \vdots \\ i_{\max} \end{bmatrix}, \tag{9}$$

where $N_{\mathrm{c}} \leq N$ determines for how many steps of the prediction horizon the constraints are enforced.

2) Constraints based on transformer peak-to-peak current: Another possibility is to bound i according to constraints on the peak-to-peak current of the transformer. According to (2), the current through the leakage inductance, i.e. the primary side of the transformer, is a function of the phase shift. Thus, for a given maximum transformer peak-to-peak current $I_T^{\max}$, the maximum and minimum phase shift are

$$\varphi_{\max} = \Phi,\ \varphi_{\min} = -\Phi, \tag{10}$$

where

$$\Phi = \begin{cases} \left(\frac{L_{\mathrm{lk}}}{2Nv_{\mathrm{o}}t_{\mathrm{s}}}\right) I_T^{\max} - \left(\frac{V_{\mathrm{i}} - Nv_{\mathrm{o}}}{4Nv_{\mathrm{o}}}\right) & \text{if } V_{\mathrm{i}} \geq Nv_{\mathrm{o}}, \\ \left(\frac{L_{\mathrm{lk}}}{2V_{\mathrm{i}}t_{\mathrm{s}}}\right) I_T^{\max} - \left(\frac{Nv_{\mathrm{o}} - V_{\mathrm{i}}}{4V_{\mathrm{i}}}\right) & \text{if } V_{\mathrm{i}} < Nv_{\mathrm{o}}. \end{cases} \tag{11}$$

In this case, the bounds on the phase shift, depend nonlinearly on the output voltage, resulting in nonlinear inequality constraints. This would render the optimization problem more difficult to solve. However, if the constraints on the current source were to be enforced only on the first step of the prediction horizon, then the bounds on the phase shift depend only on the measurement of v_o, and the bounds on φ can be easily determined from (11). With the bounds on φ, the bounds on the current source i can be determined from (8). Then, the inequality constraints for the QP problem are written as

$$\begin{bmatrix} -u(k_i) \\ u(k_i) \end{bmatrix} \leq \begin{bmatrix} -i_{\min} \\ i_{\max} \end{bmatrix}. \tag{12}$$

III. Simulation Results

A simulation study was performed to evaluate the CCS-MPC controller. The details of the simulation are discussed in Section III-A. For this study, three different controllers were designed, each with a different control frequency but same bandwidth. Their design is discussed in Section III-B. The response of the controller was evaluated for two cases: steps in the power of the load, and steps in the voltage reference of the converter. The simulation study considers constraints on the phase shift only, and constraints on the peak-to-peak current of the transfomer, discussed in Sections III-C and III-D; respectively. Moreover, it is assumed that the load of the converter is a CPL, with a bandwidth of 5 kHz.

TABLE I
Parameters used for simulation of the DAB converter.

Parameter	Value
Input voltage	350 V
Output voltage	650 V
Output capacitor (C_{o})	225 µF
Output capacitor series resistance (R_{Co})	1.57 mΩ
Switching frequency	50 kHz
Transformer turns ratio ($\mathrm{N_p/N_s}$)	7 : 12
Leakage inductance (placed on secondary – L'_{lk})	46.8 µH
Transformer magnetizing inductance	503 µH
Primary equivalent series resistance ($R_{\mathrm{esr,p}}$)	1.1 mΩ
Secondary equivalent series resistance ($R_{\mathrm{esr,s}}$)	80 mΩ
Primary switch on resistance ($R_{\mathrm{ds,p}}$)	15 mΩ
Primary switch on resistance ($R_{\mathrm{ds,s}}$)	25 mΩ
Input voltage sensor range and resolution	0–500 V, 12 bits
Output voltage sensor range and resolution	0–900 V, 12 bits
Output current sensor range and resolution	±30 A, 12 bits

Table I shows the parameters of the DAB assumed in this study. These parameters are based on the prototype of a 20 kW DAB currently under development. Parasitics of the converter are included in the simulation but not in the reduced-order model (3) used for control design.

A. Simulation study

The controller was verified using a a processor-in-the-loop (PiL) scheme [16]. In this scheme, the DAB, including modulator and analog-to-digital converters (ADCs), is simulated in a computer, the controller is implemented in the real target, and simulation and controller exchange measurements and control signals at every sample time of the controller.

The DAB was simulated using PLECS. A zero-mean white noise signal was added to the output of the voltage and current sensors, with standard deviation of 0.25 V for the voltage measurements, and 0.15 A for the current measurement. One ADC was added to each measurement, with range and resolution shown in Table I. A delay of one control period was added to the input of the modulator, to simulate the output update delay of the real hardware.

The controller was implemented in a Zynq-7000 System-on-a-Chip (SoC). To run the MPC algorithm on the target hardware, Hildreth's QP procedure was used as the QP solver [19]. The solver was executed on the hardware with a fixed number of iterations for each controller, which were determined through offline simulations. To simplify the optimization problem, the constraints were enforced only on half the steps of the prediction horizon of each design.

B. Design of the MPC controller

The MPC controller is designed according to the procedure proposed in [20]. The design of the controller consists of defining the desired controller bandwidth, and then determining the

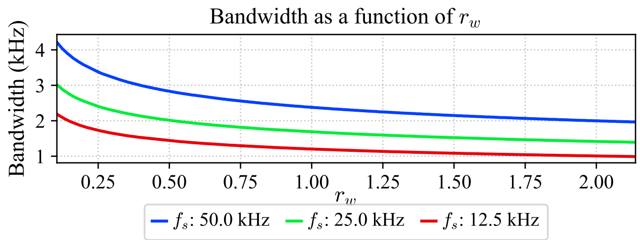

Fig. 4. Bandwidth of the unconstrained closed-loop system, for different control frequencies and horizon of $N = 40$.

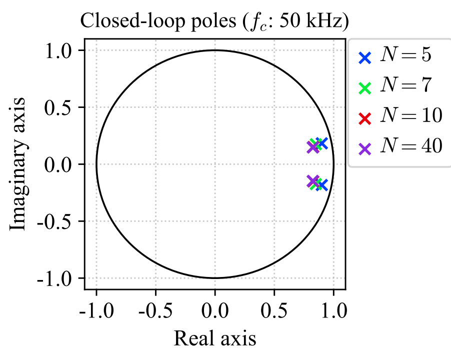

Fig. 5. Poles of the closed-loop system, for varying prediction horizon, with $f_c = 50$ kHz and $r_w = 1.99$.

control frequency, the weighting factor r_w and the horizon N. These steps are discussed next.

In the first step, the bandwidth of the unconstrained system is defined, chosen as 2 kHz in this paper. Next, the control frequency is chosen. For comparison purposes, control frequencies of 50 kHz, 25 kHz, and 12.5 kHz are selected, while the switching frequency is fixed at 50 kHz.

Having determined the control frequency, it is possible to find the weighting factor r_w for the desired bandwidth. This parameter can be extracted from Fig. 4, which shows the bandwidth of the unconstrained closed-loop system as a function of r_w. The bandwidth of the system is obtained by first assuming a fixed and long prediction horizon; for the results of Fig. 4, a horizon of 40 was chosen.

The last step is to find a suitable prediction horizon. In the previous step, the bandwidth of the system was obtained with a long horizon, which in practice would be difficult to realize. However, a sufficiently large horizon can be chosen based on the poles of the unconstrained closed-loop system. Fig. 5 shows the closed-loop poles for different prediction horizons N, for the design with control frequency of 50 kHz. For $N = 40$ and $N = 10$, the poles are almost overlapping, while they move towards the unit circle as N decreases to 7 and 5. Thus, selecting $N = 10$ gives a closed-loop behavior that is close to the case when $N = 40$. Moreover, Fig. 5 shows that shorter horizons lead to poles that are closer to the unit circle, resulting in oscillatory closed-loop responses that are observed in controllers with very short prediction horizons.

TABLE II
DESIGNED PARAMETERS FOR THE MPC CONTROLLERS.

Control freq. (f_c)	**Weight. factor** (r_w)	**Pred. horizon** (N)
50.0 kHz	1.99	10
25.0 kHz	0.513	8
12.5 kHz	0.146	6

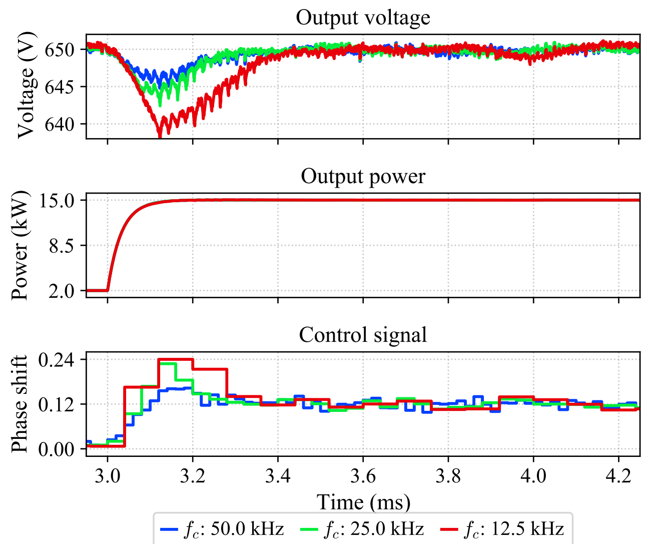

Fig. 6. Output voltage response of the different controllers for a 13 kW step in the output power.

The parameters of the designed controllers are summarized in Table II, which shows weighting factor and prediction horizon for each case of control frequency.

C. Constraints based on the phase shift

In this case, constraints are assumed only on the phase shift, assumed as $\varphi \in (-0.24, 0.24)$.

1) Load step: Fig. 6 shows the response of the closed-loop system for a 13 kW step in the output power. At higher control frequencies, the controller reacts faster to this disturbance, and thus the output voltage drop is smaller. With control frequencies of 50 kHz and 25 kHz, the voltage drop and the time to regulate the voltage back to the reference is approximately the same. At a control frequency of 12.5 kHz, the difference is more significant. Moreover, at lower control frequencies, the rate of change of the phase shift also increases. The fluctuations seen in the output voltage shown in Fig. 6 are due to nonidealities included in the model (reported in Table I).

2) Steps in the reference voltage: Fig. 7 shows the response of the closed-loop system for a 5% step in the reference voltage at an output power of 15 kW. In Fig. 7, the exact moment that the reference changed was slightly adjusted for each controller. This adjustment was made to compensate the control delay that is different for each controller, so that the change in the output voltage would be synchronized.

As Fig. 7 shows, the response of the output voltage is similar for the different controllers, although their control frequency

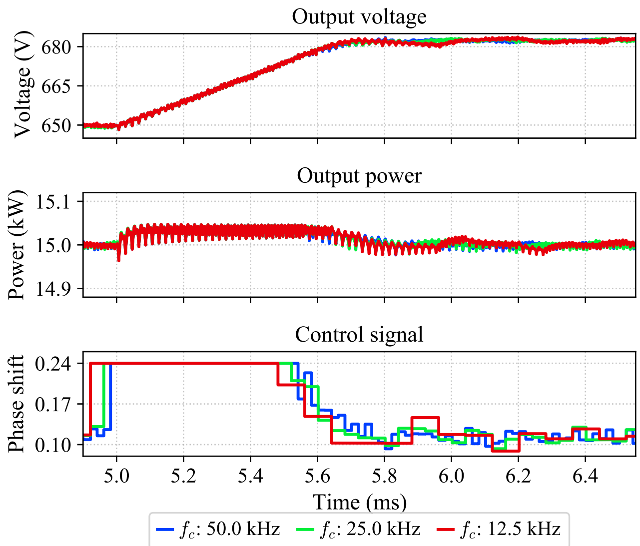

Fig. 7. Output voltage response of the different controllers for a 32.5 V step in the reference voltage.

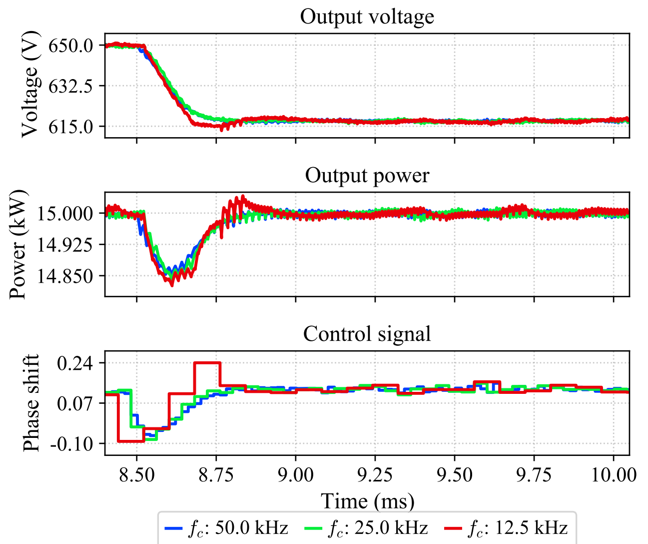

Fig. 8. Output voltage response of the different controllers for a -32.5 V step in the reference voltage.

TABLE III
HARDWARE IMPLEMENTATION OF THE CONTROLLERS.

f_c (kHz)	r_w	N	N_c	N_{iter}	t_{exec} (µs)	t_c(µs)
50.0	1.99	10	5	20	27.1	20
25.0	0.513	8	4	10	11.1	40
12.5	0.146	6	3	10	8.06	80

is different. The controllers are able to drive the output voltage to the new reference while supplying the CPL. Furthermore, the controllers respect the constraints imposed in the phase shift. Due to these physical constraints, the controller is not able to meet the designed bandwidth of 2 kHz.

Fig. 8 shows the closed-loop response for a -5% step in the reference voltage at an output power of 15 kW. The response of the controllers is also similar in this case, despite the different control frequencies. As the bounds on the phase shift are not reached in this case, the system is able to meet the designed bandwidth of 2 kHz. The faster change in the output voltage also causes a stronger disturbance on the CPL, such that its power drops momentarily before settling back to 15 kW.

3) Real-time implementation: Table III summarizes the parameters and execution time of each controller. In Table III, N_c is the number of steps of the prediction horizon where the constraints were enforced; N_{iter} is the number of iterations of the QP solver; t_{exec} is the execution time of the controller; and t_c is the control period.

As Table III shows, when selecting a control frequency of 50 kHz, the implemented controller cannot meet the required real-time constraint, as its execution time of 27.1 µs exceeds the control period of 20 µs. For a control frequency of 25 kHz and 12.5 kHz, the controllers meet the real-time constraint and present a feasible implementation. It is interesting to note that, as the control frequency decreases, the horizon can also be decreased, leading to a smaller problem that requires fewer iterations to solve. This improves the execution time, resulting in controllers that are feasible to implement in real time.

D. Constraints on transformer peak-to-peak current

In this case, the constraints of the MPC problem are based on (11) and (12), which gives the bounds on the phase shift and the rectified current as a function of the peak-to-peak current of the transformer. Because these constraints are nonlinearly related to the output voltage, they are only enforced in the first step of the prediction horizon. To show the effects of having constraints on the transformer current, only the results from the controller with a control frequency of 25 kHz are presented. Moreover, the bound on the peak-to-peak current of the transformer was set to 170 A.

Fig. 9 shows the response of the output voltage for a change in the reference voltage at an output power of 15 kW, both when there are no constraints on the transformer current, and when these constraints are imposed. When there are no constraints on the peak-to-peak current, the only active constraint is on the maximum allowable phase shift. However, as Fig. 9 shows, the peak-to-peak transformer current can be considerable during the shown transient.

When constraints on the peak-to-peak current are considered, the bounds on the maximum allowable phase shift are dynamically set according to (11). As Fig. 9 shows, the phase shift is continuously adjusted during the transient, such that the peak-to-peak current of the transformer is limited. Note that it is the peak-to-peak and not peak current that is limited. Furthermore, as shown in Fig. 9, the output voltage transient is affected by the constraint on the transformer current. With a lower bound on the phase shift, the rectified current on the secondary bridge is also lower, and it takes longer to charge the output capacitor.

 DOI 10.1109/ICDCM63994.2025.11144644

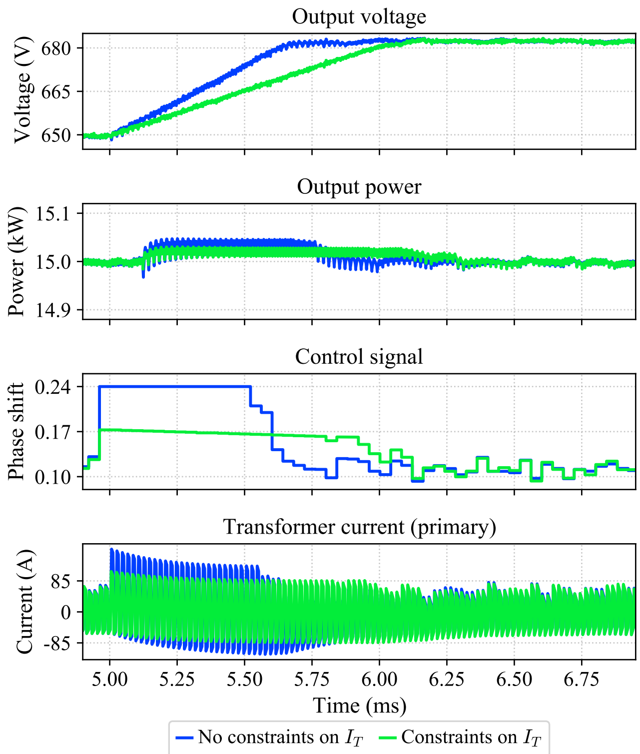

Fig. 9. Output voltage response of the closed-loop system for a 32.5 V step in the reference voltage and constraints on the peak-to-peak current of the transformer.

IV. Conclusions

This paper presented the design of an CCS-MPC controller for voltage control of the DAB. The controller is based on the reduced-order model of the DAB, and is able to control the converter while meeting some of it is physical constraints, namely limits on the phase-shift and on the transformer peak-to-peak current. The real-time feasibility of the controller is demonstrated using a PiL study, where the a CCS-MPC controller is designed for a 50 kHz DAB, and the controller achieves a prediction horizon of 8 steps when implemented in a Zynq-7000 SoC.

Future developments will look at using other modulation techniques, such as double or triple phase shift, where the additional degrees of freedom can be systematically handled with MPC.

V. Acknowledgment

This research was made possible by funding from the Carl-Zeiss-Stiftung.

References

[1] S. Ullah, A. M. Haidar, P. Hoole, H. Zen, and T. Ahfock, "The current state of distributed renewable generation, challenges of interconnection and opportunities for energy conversion based DC microgrids," *J. Clean. Prod.*, vol. 273, p. 122777, 2020.

[2] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC microgrid protection: A comprehensive review," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2019.

[3] S. Sharma, V. M. Iyer, S. Bhattacharya, K. Zou, and J. Kikuchi, "Droop-based distributed secondary control method with reduced communication complexity for radial DC microgrids," *IEEE J. Emerg. Sel. Top. Ind. Electron.*, vol. 4, no. 3, pp. 969–981, 2023.

[4] W. Xie, M. Han, W. Cao, J. M. Guerrero, and J. C. Vasquez, "System-level large-signal stability analysis of droop-controlled DC microgrids," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4224–4236, 2021.

[5] E. L. Carvalho, A. Sidorova, A. Blinov, A. Chub, and D. Vinnikov, "Design considerations of dual-active bridge DC grid-forming converter for DC buildings," *IEEE Trans. Ind. Electron.*, pp. 1–11, 2023.

[6] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, 2020.

[7] A. A. Ahmed, B. K. Koh, and Y. I. Lee, "A comparison of finite control set and continuous control set model predictive control schemes for speed control of induction motors," *IEEE Trans. Ind. Inform.*, vol. 14, no. 4, pp. 1334–1346, 2018.

[8] M. Guerreiro, S. Kharade, P. dos Santos, and S. Liu, "Power electronics control with system-on-a-chip-based platforms," in *20th IEEE PEMC*, 2022, pp. 353–359.

[9] L. Tarisciotti, L. Chen, S. Shao, T. Dragičević, P. Wheeler, and P. Zanchetta, "Finite control set model predictive control for dual active bridge converter," *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 2155–2165, 2022.

[10] L. Chen, F. Gao, K. Shen, Z. Wang, L. Tarisciotti, P. Wheeler, and T. Dragičević, "Predictive control based DC microgrid stabilization with the dual active bridge converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8944–8956, 2020.

[11] L. Chen, S. Shao, Q. Xiao, L. Tarisciotti, P. W. Wheeler, and T. Dragičević, "Model predictive control for dual-active-bridge converters supplying pulsed power loads in naval DC micro-grids," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1957–1966, 2020.

[12] Y. Zhu, Y. Yang, H. Wen, J. Mao, P. Wang, X. Fan, W. Huang, Z. Zhao, S. Mekhilef, and J. Rodriguez, "Model predictive control with a novel parameter identification scheme for dual-active-bridge converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 11, no. 5, pp. 4704–4713, 2023.

[13] J. Saeed and A. Hasan, "Unit prediction horizon binary search-based model predictive control of full-bridge DC–DC converter," *IEEE Trans. Control Syst. Technol.*, vol. 26, no. 2, pp. 463–474, 2018.

[14] F. Yan, M. Hua, Z. Xun, and D. Cao, "Model predictive control strategy based on Kalman filter for dual active bridge converter," *IEICE Electronics Express*, vol. 21, no. 2, 2024.

[15] N. Guennouni, A. Chebak, and N. Machkour, "Optimal dual active bridge DC-DC converter operation with minimal reactive power for battery electric vehicles using model predictive control," *Electronics*, vol. 11, no. 10, 2022.

[16] M. Guerreiro, W. Becker, P. dos Santos, and S. Liu, "An open processor-in-the-loop framework for power converter control," in *49th IEEE IECON*, 2023, pp. 1–6.

[17] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, 1991.

[18] S. Shao, L. Chen, Z. Shan, F. Gao, H. Chen, D. Sha, and T. Dragičević, "Modeling and advanced control of dual-active-bridge DC–DC converters: A review," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1524–1547, 2022.

[19] L. Wang, *Model Predictive Control System Design and Implementation Using MATLAB*. Springer, 2009.

[20] M. Guerreiro, P. dos Santos, and S. Liu, "On the design of a model predictive controller for a DC-DC buck converter," in *EPE'23 ECCE Europe*, 2023, pp. 1–8.